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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/520,866	01/11/2005	Guillaume De Cremoux	NL 020624	4457

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PHILIPS INTELLECTUAL PROPERTY & STANDARDS
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EXAMINER	
RILEY, SHAWN	

ART UNIT	PAPER NUMBER
2838	

DATE MAILED: 10/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/520,866	DE CREMOUX, GUILLAUME	
	Examiner	Art Unit	
	Shawn Riley	2838	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12,15 and 16* is/are rejected.

7)☒ Claim(s) *13,14 and 17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 January 2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *sep05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to because figure(s) 1A, 1B, 4A-C, and 5A-D fail(s) to have the label prior art. Correction is required.

2. The drawing(s) is(are) objected to because they fail to label (figure(s) 1A, 1B, 2, 4A-4D,) what the element boxes 16 15a&15b (note these types of elements are labeled properly in figure, e.g., 5A), 27, 26, 45, 46, 48, 49, are 16. Without some indication as to the content of the boxes (or preferably ansi symbols of the actual elements) it is not clear as to what the elements are and they are not explanatory to a reader as a quick method of determining the general background of the invention.

See MPEP 608.02 and 37 CFR 1.84 (o) -- **Legends**

> Suitable descriptive legends may be used, or may be required by the Examiner, where necessary for understanding of the drawing, subject to approval by the Office. They should contain as few words as possible.

Specification

3. The disclosure is objected to because of the following informalities: it is missing the titling of its sections (e.g., background of the art, summary of the invention, brief description of the drawings, etc.). Appropriate correction is required.

Claim Rejections - 35 U.S.C. § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 3718 of this title before the invention thereof by the applicant for patent.

2. Claims 1-12 and 16 are rejected under 35 U.S.C. §102(e) as being fully anticipated by Yakabe (U.S. Patent 7.088,112). Yakabe shows,[1] (in, e.g., the(ir) figures 4 and corresponding disclosure)

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1 Note claims will be addressed individually and the material in parentheses are the examiner's annotated comments. Further unless needed for clarity reasons, recited limitation(s), will be annotated only upon their first occurrence. Annotated claims begin with the phrase "As to claim". Claims that are not annotated are seen as having already had the invention(s) addressed previously in an annotated claim and may be repeated for convenience of the applicant/examiner. Bolded words/phrases indicate rejected material based 112 paragraph rejections. Underlined words/phrases indicate objected to material. For method claims, note that under MPEP 2112.02, the principles of inherency, if a prior art device, in its normal and usual operation, would necessarily perform the method claimed, then the method claimed will be considered to be anticipated by the prior art device. When the prior art device is the same as a device described in the specification for carrying out the claimed method, it can be assumed the device will inherently perform the claimed process. In re King, 801 F.2d 1324, 231 USPQ 136 (Fed. Cir. 1986). Therefore the previous rejections based on the apparatus will not be repeated.

As to claim 1. Capacitive feedback circuit, comprising: a voltage input terminal (Vin); a current output terminal (node of R2/R3); a feedback capacitor (C), having a first terminal connected to input terminal and having a second terminal connected to a high-impedance node (node shown connected to OP1 and Vout).

As to claim 2. Capacitive feedback circuit according to claim 1, further comprising: an amplifying element (OP1) having a high-impedance control terminal connected to said node; a current sensor (OP2) connected in series between said amplifying element and a first supply voltage (Vin); a bias current source (Cs) connected in series between said amplifying element and a second supply voltage (Ground).

As to claim 3. Capacitive feedback circuit according to claim 2, wherein said current sensor is part of a current-to-voltage converting feedback loop (loop is connected electrically), which has a high-impedance output terminal (Vout or output of OP2) connected to said node.

As to claim 4. Capacitive feedback circuit according to claim 3, wherein the current sensor has an output providing a current output signal (output of OP2), and wherein the feedback loop comprises a comparator, having one current input connected to said current output of the current sensor, having a second input connected to receive a reference current (that is the input to the negative terminal of OP2), and having a voltage output connected to said node.

As to claim 5. Capacitive feedback circuit according to claim 2, wherein the output terminal (Vout) is connected to the node between the amplifying element and the bias current source.

As to claim 6. Capacitive feedback circuit according to claim 2, wherein the output terminal is connected to the node between the amplifying element (OP1) and the current sensor (OP2).

As to claim 7. Capacitive feedback circuit according to claim 2, wherein the amplifying element comprises a first transistor, preferably a MOSFET, having its gate connected to said node (this is how amplifiers are designed).

As to claim 8. Capacitive feedback circuit according to claim 2, wherein the bias current source comprises a second transistor, preferably a MOSFET, having its source connected to second supply voltage, and having its gate connected to a source of accurate constant bias voltage (this is how amplifiers are designed).

As to claim 9. Capacitive feedback circuit according to claim 7, wherein the second transistor has its drain connected to the source of the first transistor (this is how amplifiers are designed).

As to claim 10. Capacitive feedback circuit according to claim 2, wherein the current sensor comprises a combination of two transistors, preferably MOSFETs, connected in a current mirror configuration (this is how amplifiers are designed).

As to claim 11. Capacitive feedback circuit according to claim 7, wherein the current sensor comprises a third transistor having its source connected to first supply voltage and having its drain connected to the drain of the first transistor, and further comprises a fourth transistor having its source connected to first supply voltage and having its gate connected to the gate and to the drain of the third transistor (this is how amplifiers are designed).

As to claim 12. Capacitive feedback circuit according to claim 2, wherein the comparator comprises a combination of two transistors, preferably MOSFETs, connected in a current mirror configuration (this is how amplifiers are designed).

As to claim 16. Voltage regulator comprising a capacitive feedback circuit according to claim 1 (the circuit of Yakabe is a regulating circuit, that is part of the reason it has feedback).

Note that applicants are presumed to have knowledge of their art and therefore may be expected to recognize, e.g., what a amplifier would be. Further, differences should be pointed out not between disclosure and the prior art but what is claimed and the prior art. The rejection of the instant invention did not rely on the disclosure but the claims in light of the disclosure. That is, the rejection is based heavily on what the claims state and not solely on what the disclosure discloses. As recited, the claims are anticipated by the disclosure of the prior art.

Allowable Subject Matter

3. Claims 13-14 and 17 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

4. As allowable subject matter has been indicated, applicant's response must either comply with all formal requirements or specifically traverse each requirement not complied with. See 37 C.F.R. § 1.111(b) and section 707.07(a) of the M.P.E.P.

5. The following is an examiner's statement of reasons for allowance: As to claim 13, no prior art uncovered anticipates or renders obvious applicant(s) claimed Capacitive feedback circuit including its drain connected to the drain of the fourth transistor, and further comprises a sixth transistor having its source connected to second supply voltage and having its gate connected to the gate and to the drain of the fifth transistor.

Further, as to claim 17, no prior art uncovered anticipates or renders obvious applicant(s) claimed circuit including having its drain connected to the output terminal; current coupling means coupled between the drain of said input transistor and the gate of said output transistor; wherein said current coupling means preferably comprise: two transistors, preferably MOSFETS, connected in current mirror configuration, wherein one transistor has its source connected to a second supply voltage level and has its drain connected to the drain of the input transistor, and wherein the other transistor has its source connected to said second supply voltage level, has its drain connected to a first bias current source and to the gate of said output transistor, and has its gate connected to the gate and to the drain of the said one transistor; an output current sensor associated with the output transistor, providing a sensor output current signal representing the

output current; wherein the output current sensor preferably comprises a sensor transistor of the same conductivity type as the output transistor, having its source and gate connected in parallel to the source and gate of the output transistor; a current feedback loop feeding back a signal derived from the sensor output current signal to control said controllable impedance; wherein the current feedback loop preferably comprises: two transistors, preferably MOSFETS, connected in current mirror configuration, wherein one transistor has its drain connected to receive said sensor output current signal and wherein the other transistor has its drain connected to the source of the input transistor.

Conclusion

Any inquiry from other than the applicant/attorney of record concerning this communication or earlier communications from the Examiner should be directed to the Patent Electronic Business Center (EBC) at 1.866.217.9197. Any inquiry from a member of the press concerning this communication or earlier communications from the Examiner or the application should be directed to the Office of Public Affairs at 703.305.8341. Any inquiry from the applicant or an attorney of record concerning this communication or earlier communications from the Examiner should be directed to Examiner Riley whose telephone number is 571.272.2083. The Examiner can normally be reached Monday through Thursday from 7:30-6:00 p.m. Eastern Standard Time. The Examiner's Supervisor is Karl Easthom who can be reached at 571.272.1989. Any inquiry about a case's location, retrieval of a case, or receipt of an amendment into a case or information regarding sent correspondence to a case **should be directed to 2800's Customer Service Center** at 571.272.2815. Any papers to be sent by fax MUST BE sent to fax number **571-273-8300**. Any inquiry of a general nature of this application should be **directed to the Group receptionist** whose telephone number is 571.272.2800. Status information of cases may be found at http://pair-direct.uspto.gov wherein unpublished application information is found through private PAIR and published application information is found through public PAIR. Further help on using the PAIR system is available at 1.866.217.9197 (Electronic Business Center).

October 06

Shawn Riley
Primary Examiner